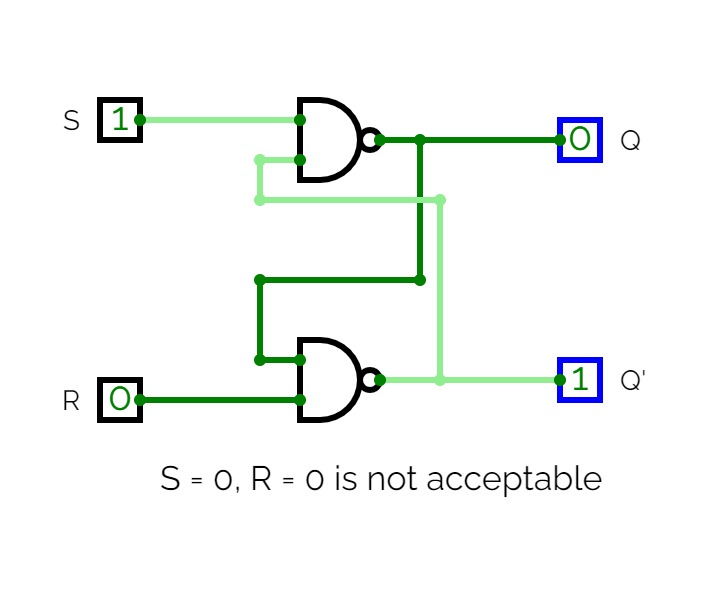
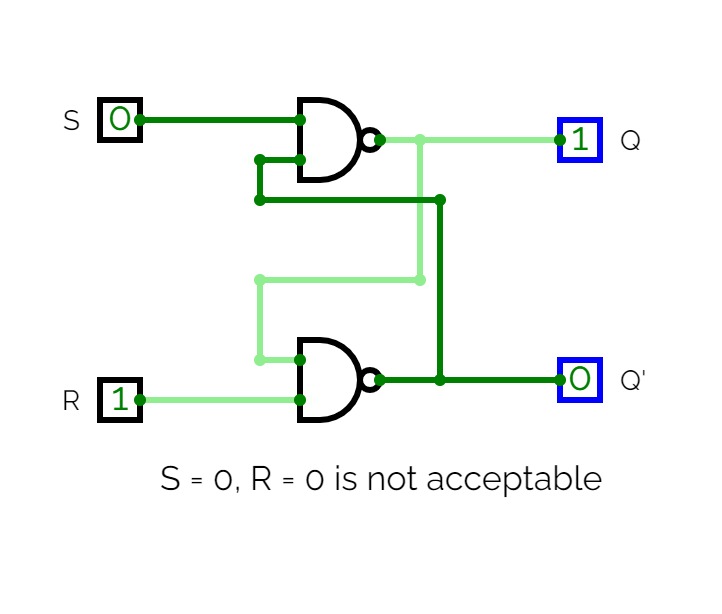
**Assignment 6**

**Name – SURAJ KUMAR YADAV**

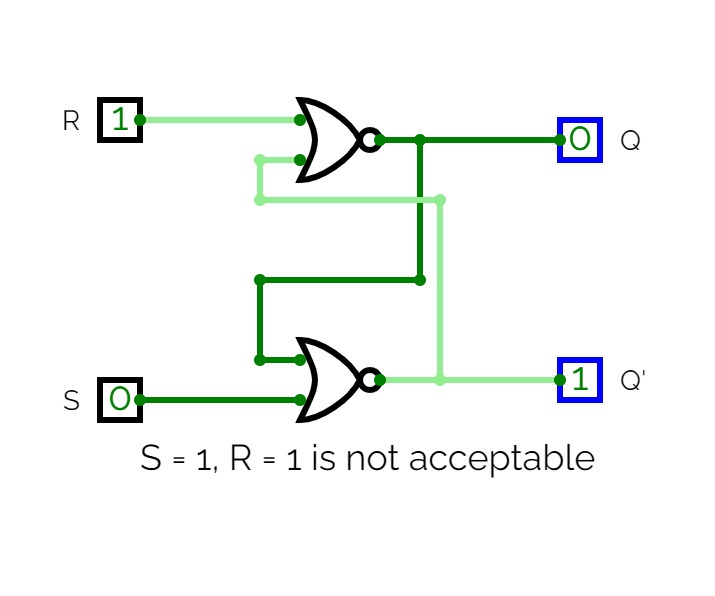
**ROLL NO. – 20220PHY014**

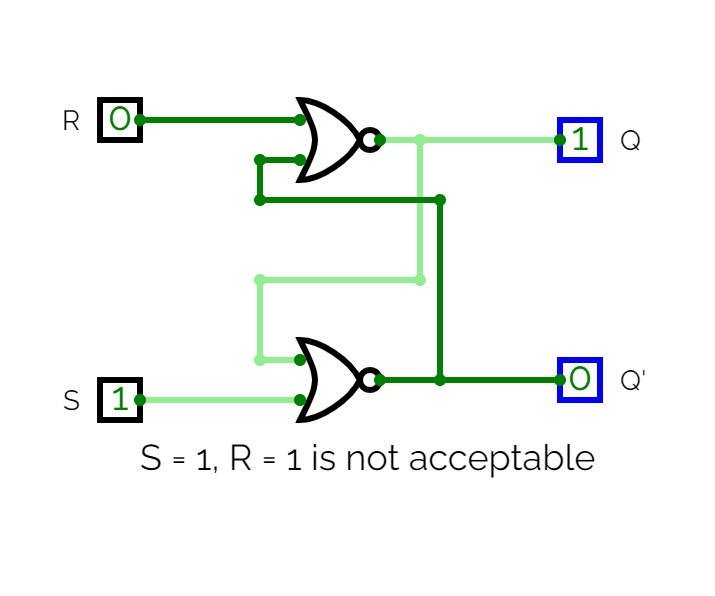
1. **Design a SR latch using NAND gates**

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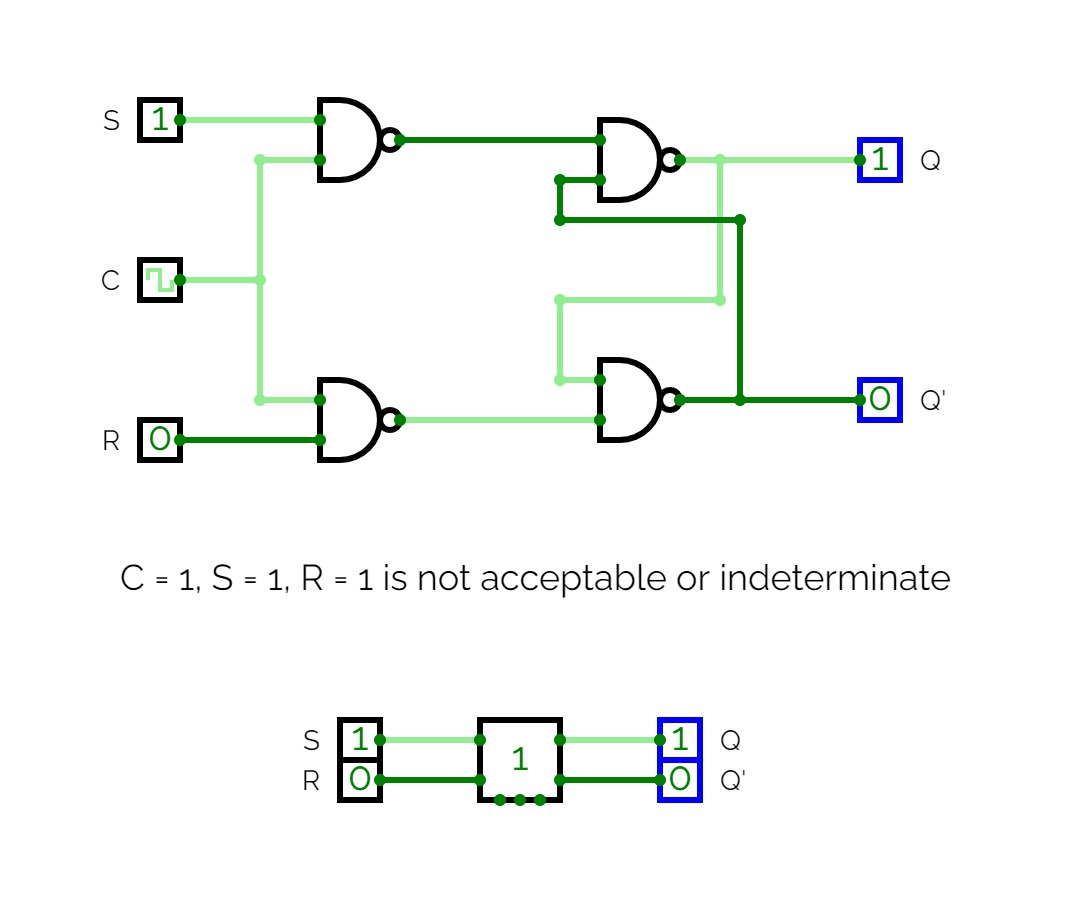
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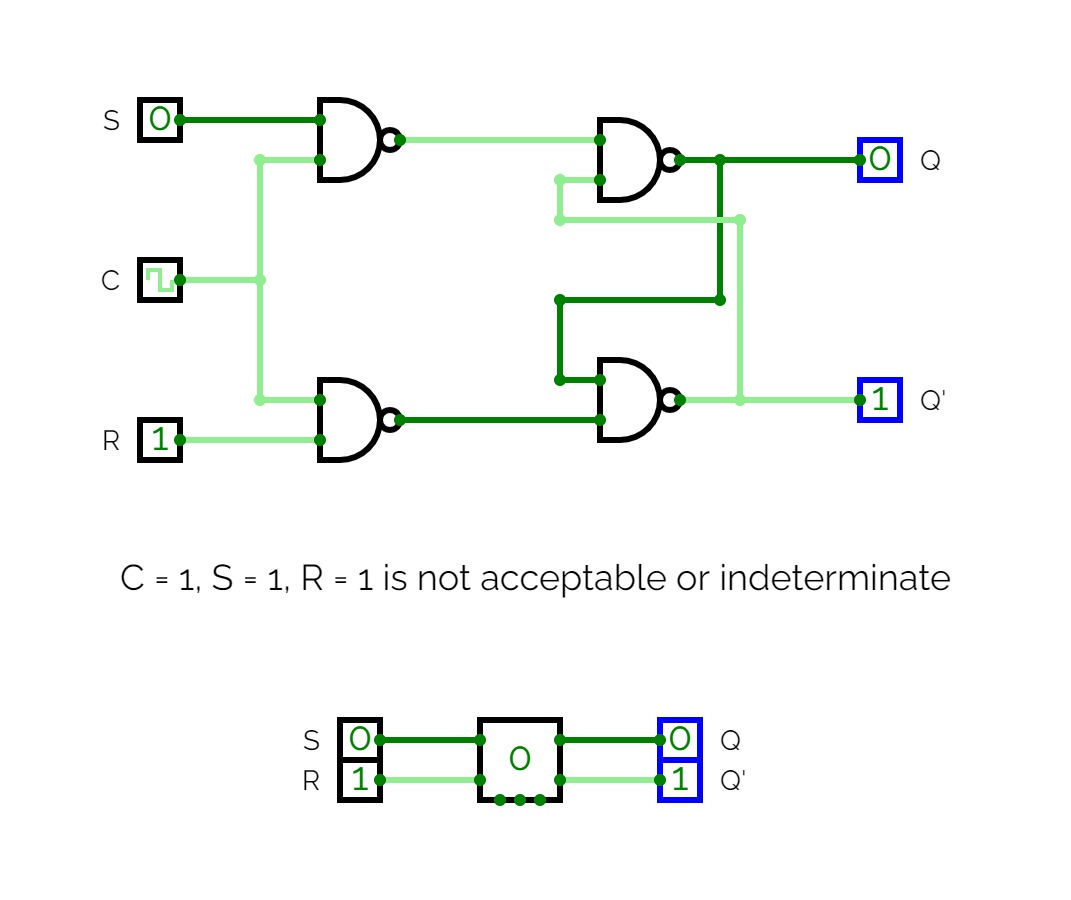
1. **Design a SR latch using NOR gates**

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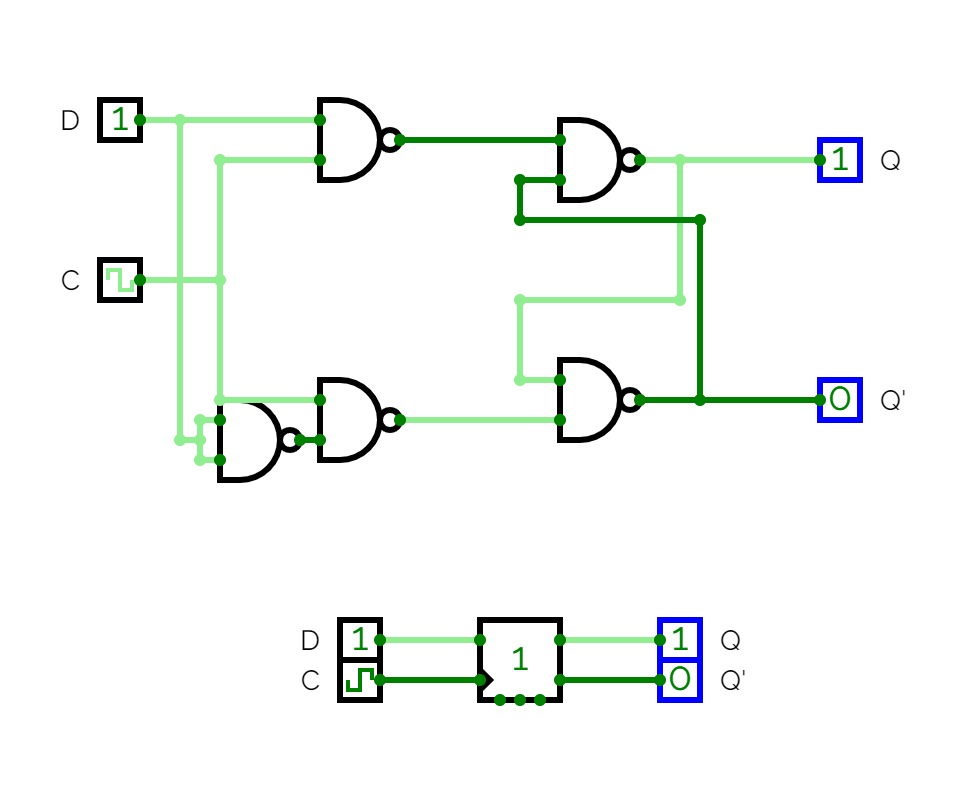
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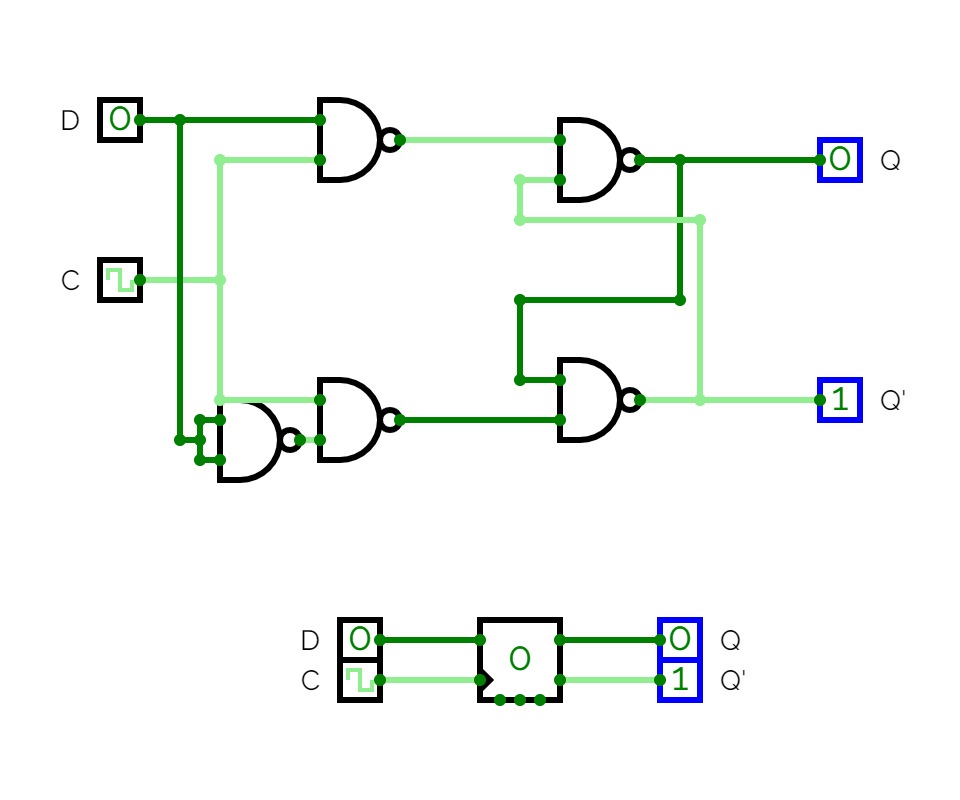
1. **Design SR latch with control input using NAND gates**

****

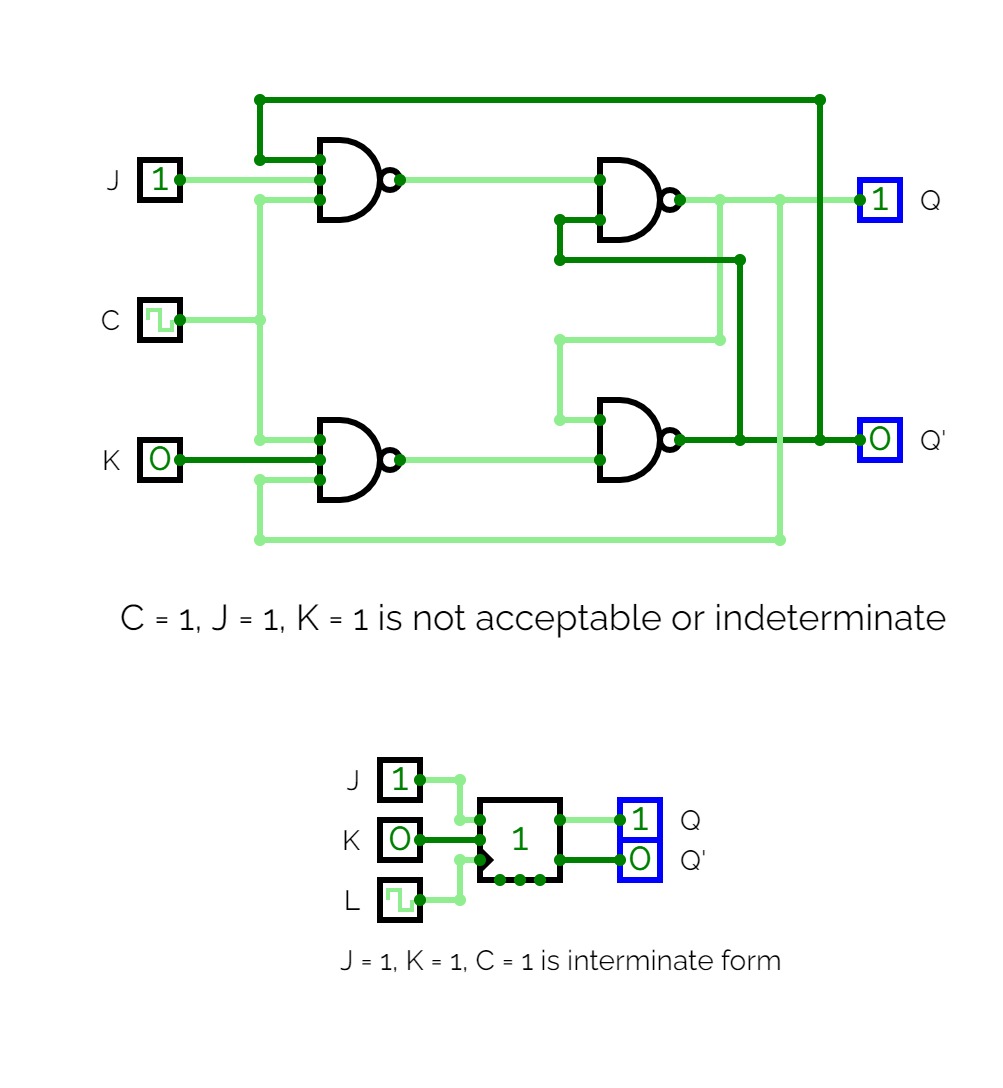
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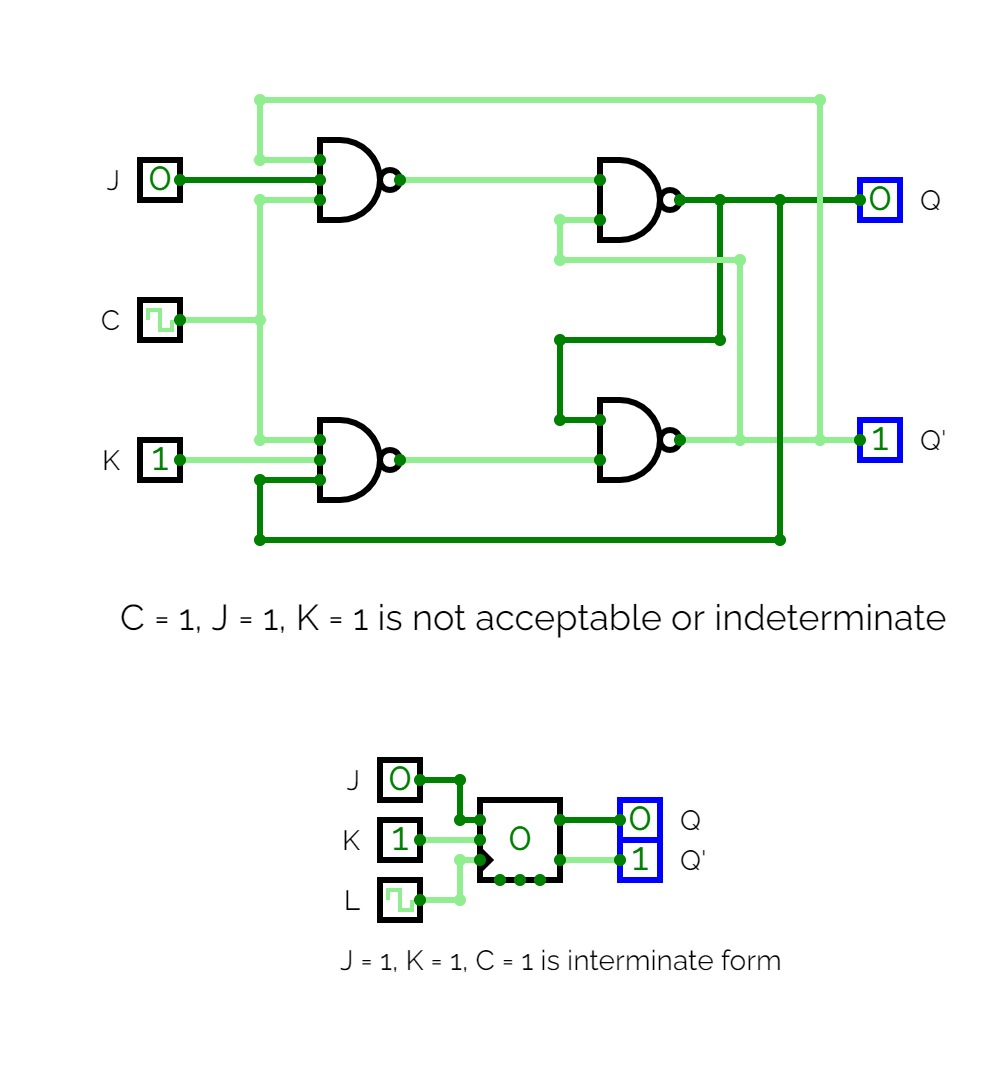
1. **Design D flip flop using NAND gate**

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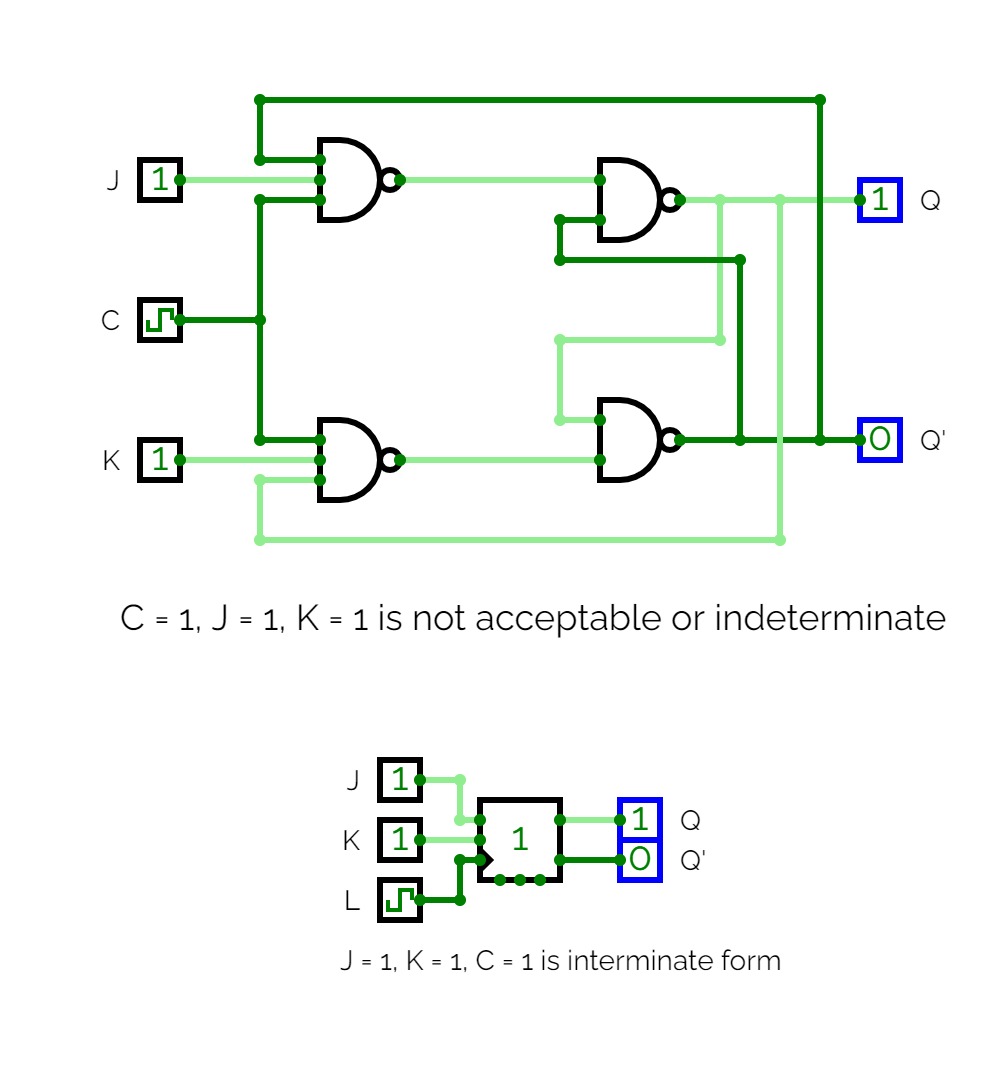
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1. **Design JK flip flop using NAND gate and show the race around condition**

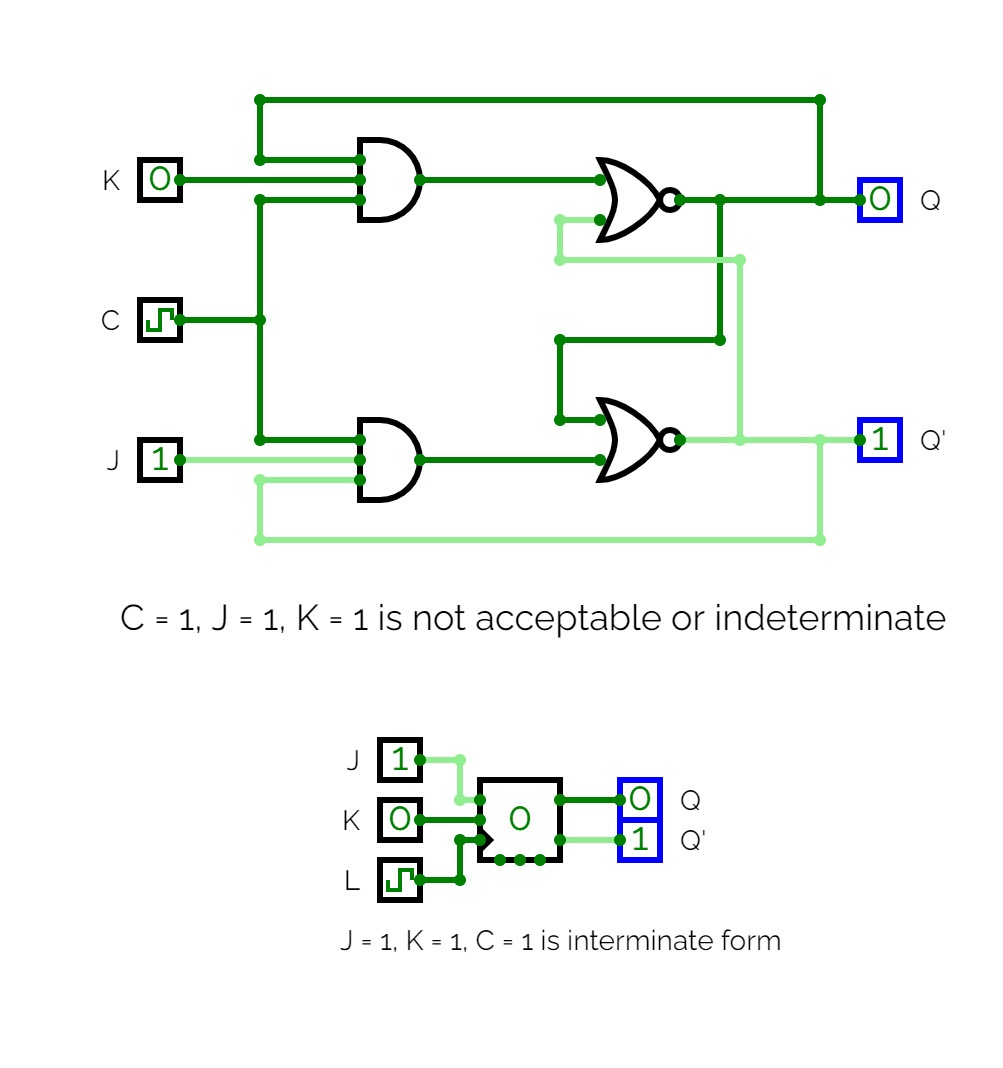
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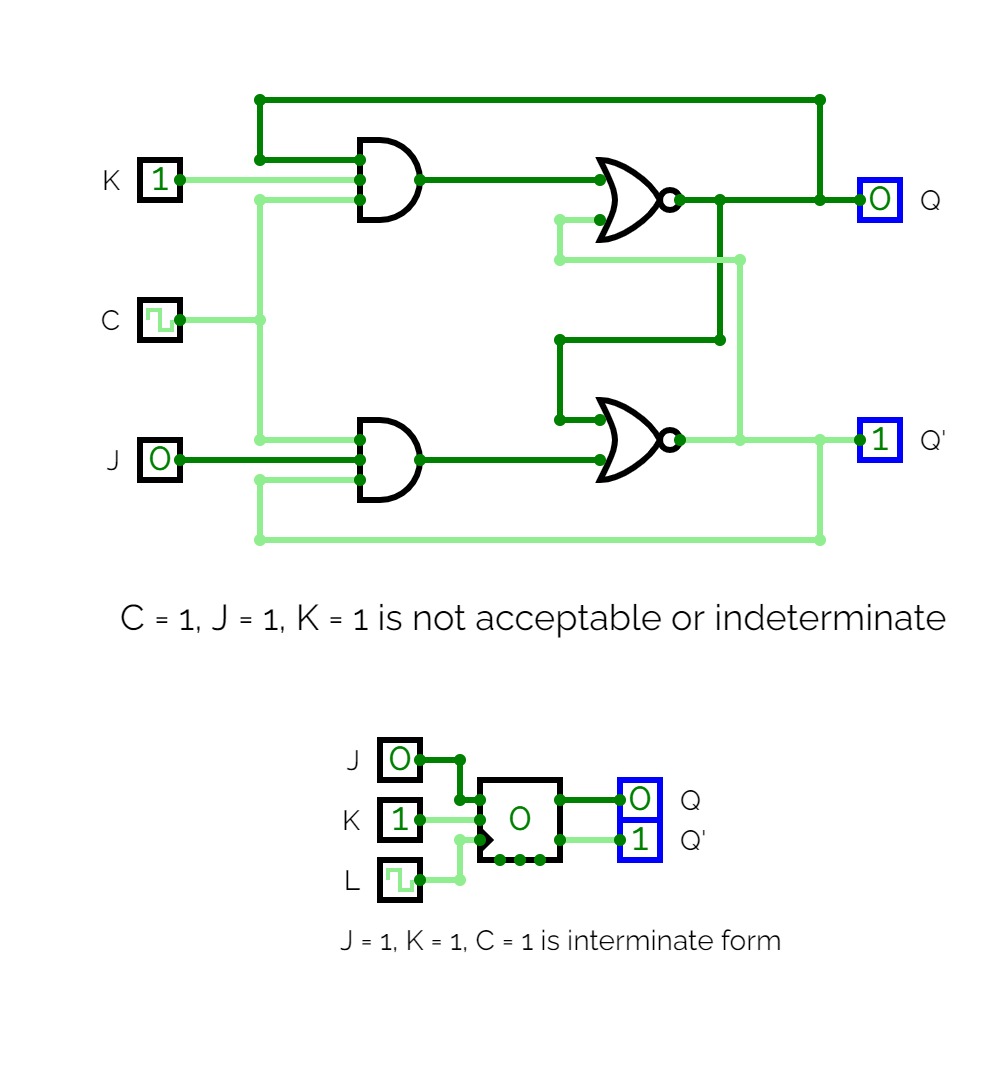
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1. **Race around condition**

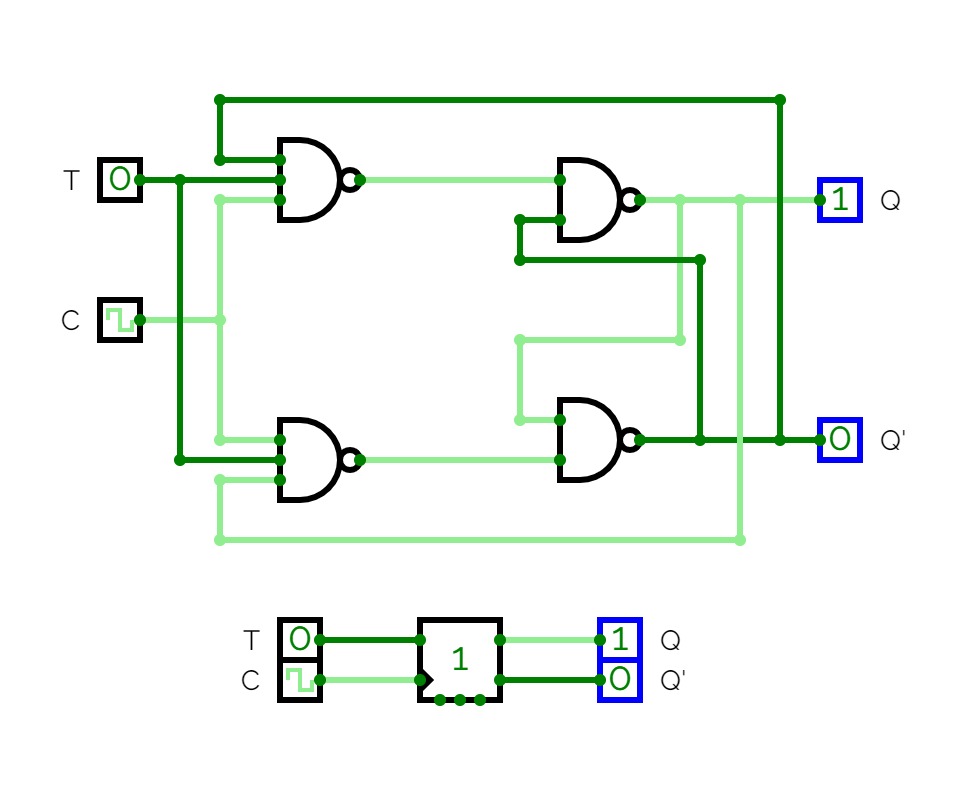
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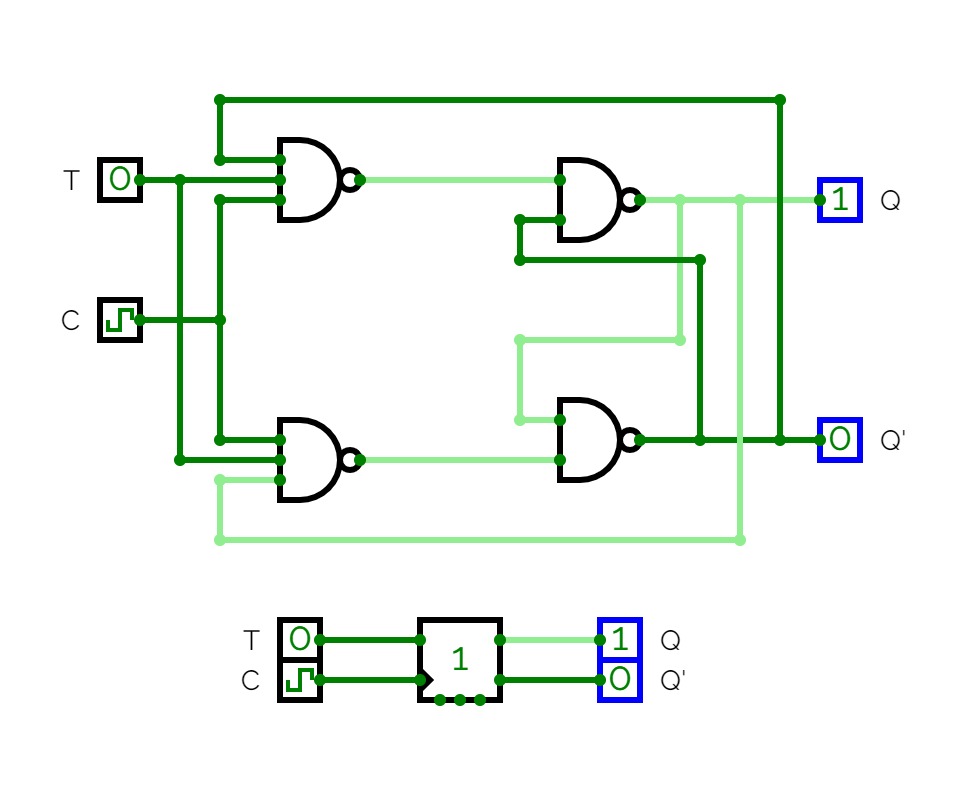
1. **Design JK flip flop using AND and NOR gates**

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1. **Design T flip flop using NAND gates**

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